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EXAMINER
PLANTE, JONATHAN R

ART UNIT	PAPER NUMBER
2182	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,103	SMITH ET AL.	
	Examiner	Art Unit	
	JONATHAN R. PLANTE	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8 and 10-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8 and 10-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the Applicant's communication filed 08/29/2008 in response to PTO Office Action mailed 06/22/2007. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

Drawing Amendments

2. Acknowledgement of receiving replacement drawings, which were received by the Office on 08/29/2008. These drawings are Figures 1 and 2.

The objections to the drawings have been withdrawn due to amendment filed on 08/29/2008.

Specification Amendments

3. Acknowledgement of receiving amendments to the specification, which were received by the Office on 08/29/2008. The amendments to the specification included (Page 2, Lines 11-15), (Page 7, Lines 3-10), and (Page 8-9, Lines 16-7). The specification has been updated according to reflect amendments.

The objections to the specification have been withdrawn due to amendment filed on 08/29/2008.

Claim Amendments

4. Acknowledgment of receiving amendments to the claims, which were received by the Office on 08/29/2008. Claims 8, 10-13 are amended, claims 1-7, 9, and 14-15 are canceled, and there are no new claims.

The 35 USC § 112 rejections to the Claims have been withdrawn due to amendment filed on 08/29/2008.

Response to Arguments

In response to Applicant's arguments concerning the rejection of Claims 8 and 11-13 in respect to Benis (US 2003/0125916) the Examiner provides the following comments:

a. On page 10 of remarks filed 08/29/2008 the Applicant makes the statement "To 'simulate the array of flip flops and in particular to model metastable effects, three registers 480, 482 and 484 are defined for simulation of the circuit only (that is, these registers are not used for synthesis of the circuit).'". The Examiner points out that the current claim language is only directed to "Simulation system for simulation of an electronic circuit" (Claim 9, Line 1). The claim language is only directed to simulation and nowhere in the claim language is the term "synthesis" used or implicated. The Examiner also refers to Benis " The present invention allows synthesis to be selectively turned on and off during simulation. The present invention also introduces a feature in which simulation can be

selectively turned on and off during synthesis." (Paragraph 0016), "In summary, the present invention can be used to simulate the functionality of one or more metastable flip flops. The present invention can also be used to synthesize flip flops. Thus, the same software module can be used for both synthesis and simulation." (Paragraph 0017), and "In the present embodiment, the registers 480, 482 and 484 are defined in addition to other registers that may be defined for synthesis. The size of the registers 480, 482 and 484 is a function of the width of the array." (Respect to Figure 4A).

b. In response to Applicant's argument concerning the placement of the Registers 480, 482, and 484 and multiplexer 460 the Examiner is not persuaded. The Examiner notes the simulated metastable boundary is between the first rank and second rank of flip flops where the metastable boundary indicates the boundary between the asynchronous clock domains. If one is to extend the metastable boundary line down to the multiplexer 460 the multiplexer's left side is incident with the metastable boundary indicating that the multiplexer is in the second clock domain, further register 484 is clear to the right of the metastable boundary and is inside the second clock domain. Where the register 484 is a jitter element. Additionally the Examiner refers Applicant to paragraph 0033 that reads as "Although the metastable boundary is shown as occurring between the first and second ranks, it will be seen that the metastable boundary can be simulated between any two ranks of flip flops. For synthesis, the metastable boundary is in actuality at the input to the first rank of flip flops". Where Registers

480, 482, and 484, Mux 460, and Random Number Generator 470 are clearly in the second clock domain since they would be to the right of the metastable boundary according to paragraph 0033.

However, the Examiner has changed the rejection in respect to Benis from 35 USC 102 to a 35 USC 103 rejection below rendering Applicant's arguments moot.

In response to Applicant's arguments concerning the rejection of Claims 8 and 10, and 12-13 in respect to Sharma et al. (US 6,598,191 B1) the Examiner is not persuaded.

a. Figure 7 as Applicant has acknowledged and pointed out on page 13 of remarks that jitter elements have been inserted in the read domain (second clock domain). Applicant argues however that the jitter elements of Figure 7 do not jitter data from the write domain. The Examiner is not persuaded. In reviewing Figure 7 the Examiner directs Applicant to "INPUT 1" (38) and to follow the data through the circuit. "INPUT 1" enters "WRITE FLIP-FLOP LEVEL A" (44) exits "WRITE FLIP-FLOP LEVEL A" (44) crossing the asynchronous clock boundary (36) and becoming input to "READ FLIP-FLOP LEVEL B" (52) the data then exits "READ FLIP-FLOP LEVEL B" (52) and becomes input data to both "EXTENDED FLIP-FLOP LEVEL C" (104) and "MULITPLEXER" (110). As a result the data from the write domain is jittered by jitter elements in the read domain satisfying the claim limitations as currently presented.

New Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6. **Claims 8, 10, and 12-13 are rejected under 35 U.S.C. 102(a) as being anticipated by Sharma et al. (US 6,598,191 B1 July 22, 2003).**

(Claim 8): Sharma et al. discloses:

a. Simulation system for simulation of an electronic circuit, the circuit being representable by a network of logical elements, **[*hardware emulator* (Column 2, Line 15)]** the circuit comprising

b. a first and a second asynchronous clock domain, **[*asynchronous clock domain* (Column 1, Line 18), WRITE DOMAIN (Figure 7, 32), READ DOMAIN (Figure 7, 34)]** wherein

c. jitter elements are additionally insertable in the second asynchronous clock domain at predetermined portions of circuit boundaries between the first and the second asynchronous clock domain, **[MULTIPLEXER (Figure 7, Indexes 110, 112, 114), PSEUDO- RANDOM GENERATOR (Figure 7, 102), ["EXTENDED FLIP-FLOP LEVEL C" (Figure 7, Indexes 104, 106, 108)]** the jitter elements being representable as logical elements, **[MULTIPLEXER (Figure 7, Indexes 110, 112, 114), PSEUDO- RANDOM GENERATOR (Figure 7, 102), ["EXTENDED**

FLIP-FLOP LEVEL C" (Figure 7, Indexes 104, 106, 108)] the values of which are randomly set, **[PSEUDO- RANDOM GENERATOR (Figure 7, 102)]**

d. wherein at least on of the jitter elements is configured to jitter data from the first asynchronous clock domain. **[*The Examiner has interpreted Figure 7 as depicting first asynchronous data represented as "INPUT 1" (38) entering "WRITE FLIP-FLOP LEVEL A" (44) exiting "WRITE FLIP-FLOP LEVEL A" (44) crossing the asynchronous clock boundary (36) and becoming input to "READ FLIP-FLOP LEVEL B" (52) the data then exits "READ FLIP-FLOP LEVEL B" (52) and becomes input data to both "EXTENDED FLIP-FLOP LEVEL C" (104) and "MULITPLEXER" (110).*]**

(Claim 10): Sharma et al. discloses:

a. wherein the jitter elements comprise delay elements for introducing predetermined timing delays which is randomly exercised **[*the delay register and multiplexer controlled by the random signal selector are used to randomly exercise the timing delay* (Column 2-3, Lines 51-5)].**

(Claim 12): Sharma et al. discloses:

a. wherein the jitter elements are interactively inserted by a user." as **[*can be inherently declared in the hardware description using Verilog or similar hardware model software.* (Column 2, Line 15-21)].**

(Claim 13): Sharma et al. discloses:

a. wherein the jitter elements are automatically inserted using predetermined modules **[*the module consisting of the delay register, multiplexer, and random generator can be inserted within any clock domain by the simulation for verifying the asynchronous boundary behavior as part of the simulation and verification* (Column 4, Line 44-48)].**

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 8 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Benis (US 2003/0125916 A1 July 3, 2003).**

(Claim 8): Benis teaches:

a. Simulation system for simulation of an electronic circuit, the circuit being representable by a network of logical elements, **[*simulation* (ABSTRACT)]** the circuit comprising:

b. a first and a second asynchronous clock domain, **[*asynchronous clock domain* (Paragraph 0002)]**

c. wherein jitter elements **[RANDOM NUMBER GENERATOR (Figure 4A, 470), MUX (Figure 4A, 460), Register (Figure 4A, 484)]** are additionally insertable in the second asynchronous clock domain at predetermined portions of circuit boundaries between the first and the second asynchronous clock domain, **[RANDOM NUMBER GENERATOR (Figure 4A, 470), MUX (Figure 4A, 460), Register (Figure 4A, 484)** ***Where the Examiner has interpreted these elements being in the second clock domain and Register (Figure 4A 484) is clearly in the second clock domain with being entirely to the right of the metastable boundary.*****]**

d. the jitter elements being representable as logical elements, **[*multiplexers and registers* (Paragraph 0036)]** the values of which are randomly set, **[*random number generator* (Figure 4A, 470)]**

e. wherein at least one of the jitter elements is configured to jitter data from the first asynchronous clock domain. **["In the present embodiment, the simulation of the array with metastable effects also includes a simulated multiplexer (MUX) 460 that receives inputs from registers 480 and 482, multiplexes those inputs, and provides outputs to register 484. In this embodiment, MUX 460 multiplexes the inputs from registers 480 and 482 responsive to a pattern generator. In one embodiment, for simulation, a random number generator 470 is coupled to the simulated MUX 460; however, a random number generator is just one implementation of a pattern generator, and other types of pattern generators may be used. The functionality of the**

MUX 460 and random number generator 470 is further described below." (Paragraph 0036), ***Where the Examiner has interpreted the above and in respect to Figure 4A, as registers 480 and 482 receive data from the first clock domain (Registers 480 and 482 are to the left of the metastable boundary) and provide the data to the Multiplexer (460) and Register (484) that are to the right of the metastable boundary indicating that they are in the second clock domain.*** **]**

Further in view of the rejection above, it is obvious to one skilled in the art that the jitter elements (multiplexer 460, random number generator 470, and register 484) are in the second clock domain since the metastable condition being tested or simulated occurs in the second clock domain when data crosses an asynchronous clock domain. The motivation to have the jitter elements in the second clock domain is for the jitter elements to be synchronized with the second clock domain where the clock of the second clock domain controls the latches so that metastable states can be simulated and induced for accurate testing of the circuits' ability to recover from a metastable signal. Further a metastable condition can not occur in the first clock domain since data is being outputted from the first clock domain to the second clock domain where the input to the latches in the first clock domain are contained within the first clock domain also. As a result since the metastable condition occurs in the second clock domain is it obvious to have the metastable inducing logic in the second clock domain.

Additionally the Examiner refers Applicant to paragraph 0033 that reads as "Although the metastable boundary is shown as occurring between the first and second ranks, it will be seen that the metastable boundary can be simulated between any two ranks of flip flops. For synthesis, the metastable boundary is in actuality at the input to the first rank of flip flops". Where Registers 480, 482, and 484, Mux 460, and Random Number Generator 470 are clearly in the second clock domain since they would be to the right of the metastable boundary according to paragraph 0033.

Examiner Note: Further in view of the teachings of Benis it would have been obvious to one skilled in the art to perform a mere rearrange the parts/elements to perform the same functionality.

(Claim 11): Benis teaches:

a. wherein the jitter elements comprise x generator elements for introducing predetermined signal values which are randomly generated **[RANDOM NUMBER GENERATOR" (Figure 4A, 470)].**

(Claim 12): Benis teaches:

a. wherein the jitter elements are interactively inserted by a user **[*user is capable of entering information and performing command selections via a user interface and input device* (Paragraph 0027)].**

(Claim 13): Benis teaches:

a. wherein the jitter elements are automatically inserted using predetermined modules." as **[*multiplexers 460, 480, and 482 in addition to the random number generator are simulated by the simulation* (Paragraph 0036) *and it is inherent that the simulation program inserts these simulation for each asynchronous interface to test for metastability*].**

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONATHAN R. PLANTE whose telephone number is

(571)272-9780. The examiner can normally be reached on Monday -- Thursday 10:00 AM to 4:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tariq Hafiz can be reached on (571) 272-6729. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. R. P./
Examiner, Art Unit 2182
December 3, 2008

/Ilwoo Park/
Primary Examiner, Art Unit 2182
December 3, 2008